AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate containing a first region and a second region;

first MISFETs formed in said first region;

second MISFETs formed in said second region, each of said second MISFETs having a gate electrode and impurity regions;

a first insulating layer formed over said first and second MISFETs;

word lines formed over said first region;

bit lines formed over said word lines and said first insulating layer,

wherein each of said first MISFETs is included in an individual one of plural memory cells, each of said memory cells being connected to one of said bit lines and one of said word lines;

a second insulating layer formed over said bit lines and said first insulating layer,

wherein said first and second insulating ~~layer having a hole~~ layers have holes formed therethrough;

~~a plug~~ plugs formed in said ~~hole~~ holes; and

a wiring layer formed over said second insulating ~~film~~layer, said wiring layer being electrically connected to ones of said impurity ~~region~~ regions of said second MISFETs via ones of said ~~plug~~plugs.

2. (New) A semiconductor integrated circuit device according to claim 1, wherein said plugs are formed of built-up films, respectively.

3. (New) A semiconductor integrated circuit device according to claim 2, wherein said built-up films are formed of a titanium nitride film and a tungsten film, respectively.

4. (New) A semiconductor integrated circuit device comprising:

first MISFETs formed in a first region, each of said first MISFETs at least having a source region and a drain region;

second MISFETs formed in a second region, each of said second MISFETs at least having a source region and a drain region;

at least one bit line formed over said first region;

at least one word line formed in said first region;

at least one capacitor element formed over one of said bit lines,

wherein each of said first MISFETs is included in an individual one of plural memory cells, each of said memory cells being coupled to a respective word line, a respective bit line and said capacitor element corresponding thereto;

a first insulating film interposed between said first and second

MISFETs and said at least one bit line;

a second insulating film formed over said first insulating film, said second insulating film being interposed between said at least one bit line and said at least one capacitor element; and

a wiring layer formed over said second insulating film,

wherein each of said at least one bit line is connected to one of said source and drain regions of ones of said first MISFETs corresponding thereto via one of first plugs formed in said first insulating film,

wherein each of said at least one capacitor element is connected to the other of said source and drain regions of ones of said first MISFETs corresponding thereto via a corresponding second plug formed in said second insulating film and another of said first plugs, and

wherein said wiring layer is connected to said source and drain regions of ones of said second MISFETs via respective ones of third plugs formed in said first and second insulating film.

5. (New) A semiconductor integrated circuit device according to claim 4, wherein said first plugs are formed of a poly-silicon film, respectively.

6. (New) A semiconductor integrated circuit device according to claim 4, wherein said second plug is formed of a built-up film.

7. (New) A semiconductor integrated circuit device according to claim 6, wherein said built-up film is formed of a titanium nitride film and a tungsten film.

8. (New) A semiconductor integrated circuit device according to claim 4, wherein said third plugs are formed of a built-up film, respectively.

9. (New) A semiconductor integrated circuit device according to claim 8, wherein said built-up film is formed of a titanium nitride film and a tungsten film.